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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/992,637	11/06/2001	Govind Kizhepat	GKIZ 1000-1	5830

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EXAMINER	
STEVENS, ROBERT	
ART UNIT	PAPER NUMBER
2176	

DATE MAILED: 10/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/992,637	KIZHEPAT, GOVIND	
	Examiner	Art Unit	
	Robert M. Stevens	2176	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to communications: **Application No. 09/992,637** RCE filed 7/29/2005 by Kizephat entitled "Method and Apparatus for Performing Computations and Operations on Data Using Data Steering".

2. The FAOM rejections of claims 1-33 under 35 USC 103(a) as being unpatentable over Athanas in view of Hillis, have been withdrawn as necessitated by amendment.

3. Claims 1-33 are pending. Claims 1, 12, 23 and 29 are independent.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 1-23 and 25-32 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Hillis et al. (US Patent No. US 5,590,283, filed Jan. 27, 1995 and issued Dec. 31, 1996, hereafter referred to as "Hillis") in view of McMahon (US Patent No. US 5,867,724, filed May 30, 1997 and issued Feb. 2, 1999, hereafter referred to as "McMahon").

Regarding independent method claim 1, Hillis discloses:

A data processing system, comprising:

a plurality of functional units having respective inputs and outputs, and adapted to perform respective tasks using input data at the respective inputs and to supply output data at the respective outputs, and adapted to perform respective tasks using input data at the respective inputs and to supply output data at the respective outputs, within a functional cycle; (Fig. 1, col. 6 lines 35-38)

a plurality of routing units, responsive to respective routing control signals, by which data is steered among the plurality of functional units, routing units in the plurality of routing units being coupled to respective subsets of functional units in the plurality of functional units, wherein at least one of said respective subsets is different that another of said respective subsets; (Fig. 1 , especially noting PE0 ... Pen, SP0 ... SPn and IOP0 ... IOPk, and col. 6 lines 39-51) *and*

control word distribution circuitry which supplies control words the routing control signals in parallel to the plurality of routing units to establish a route for a functional cycle . (Fig. 10D in context of Fig. 1 #15, col. 6 lines 39-51)

Hillis, however, does not explicitly disclose:

... :

... ;

... *data is steered* ... ; *and*

... .

McMahon, though, discloses:

... :

... ;

... *data is steered* ... ; (Abstract) *and*

... .

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of McMahon for the benefit of Hillis, because to do so would have allowed a designer to improve microprocessor throughput, as taught by McMahon in col. 2 lines 15-24. These references were all applicable to the same field of endeavor, i.e., computer architecture.

Regarding claim 2, which is dependent upon claim 1, Hillis discloses:

wherein said plurality of routing units includes at least one multiplexer having a plurality of inputs and coupled to respective functional units in the plurality of functional units and at least one output coupled to a functional unit in the plurality of functional, and the routing control signal for the multiplexer specifies one of a plurality of inputs to indicate a source functional unit, and one of the at least one outputs to indicate a destination functional unit. (Fig. 9B-2, especially #333, teaches the well-known use of multiplexers)

Regarding claim 3, which is dependent upon claim 1, Hillis discloses:

wherein said plurality of routing units includes at least one crossbar switch. (col. 3 line 65 – col. 4 line 10)

Regarding claim 4, which is dependent upon claim 1, Hillis discloses:

wherein said plurality of functional units includes at least one storage element. (col. 5 lines 50-67)

Regarding claim 5, which is dependent upon claim 1, Hillis discloses:

wherein said plurality of functional units includes at least one logic block which performs a plurality of available functions, and includes logic to select an output from one of the plurality of available functions in response to a routing control signal in the control. (Fig. 1, col. 6 lines 35-38)

Regarding claim 6, which is dependent upon claim 1, Hillis discloses:

wherein said plurality of functional units includes a memory responsive to addresses, write control signals, and read control signals, and the control word distribution circuitry supplies at least one of the write control signals and read control signals. (Fig. 1, col. 6 lines 35-38)

Regarding claim 7, which is dependent upon claim 6, Hillis discloses:

wherein said control word the control word distribution circuitry supplies an address for said memory. (Fig. 10D)

Regarding claim 8, which is dependent upon claim 6, Hillis discloses:

wherein an address for said memory is supplied by one of the plurality of functional units. (Fig. "9A-2B")

Regarding claim 9, which is dependent upon claim 1, Hillis discloses:

wherein functional units in the plurality of functional units comprise logic dedicated to specific processing tasks (Fig. 1, it being inherent that functional units must perform some task)

Regarding claim 10, which is dependent upon claim 1, Hillis discloses:

wherein functional units in the plurality of functional units comprise hardwired logic dedicated to specific processing tasks. (Fig. 1, it being inherent that functional units must perform some task)

Regarding claim 11, which is dependent upon claim 1, Hillis discloses:

wherein said control word logic distribution circuitry supplies said control routing control signals synchronously to the plurality of functional units. (Fig. 1 #15, noting #17)

Regarding independent method claim 12, Hillis discloses:

A data processing system, comprising:
a plurality of processing blocks having respective inputs and outputs, and adapted to perform respective processes using input data at the respective inputs

and to supply output data at the respective outputs, within a function cycle; (Fig. 1, col. 6 lines 35-38)

a plurality of routing units, responsive to respective routing control signals for the plurality of processing blocks, by which data is steered among the inputs and outputs of the plurality of processing blocks, routing units in the plurality of routing units being coupled to respective subsets of processing blocks in the plurality of processing blocks, wherein at least one of said respective subsets of processing blocks is different that another of said respective subsets processing blocks; (Fig. 1 , especially noting PE0 ... Pen, SP0 ... SPn and IOP0 ... IOPk, and col. 6 lines 39-51) *and*

block level control word distribution circuitry which supplies control words for respective function cycles to the plurality of routing units, said control words including the routing control signals for the plurality of routing units; (Fig. "11B-2D")

wherein processing blocks in said plurality of processing blocks respectively include: (Fig. "11B-2D", Fig. 1, col. 6 lines 35-38)

a plurality of functional units having respective inputs and outputs, and adapted to perform respective processes using input data at the respective inputs and to supply output data at the respective outputs, within a block function cycle; (Fig. 1, col. 6 lines 35-38)

a plurality of unit level routing units, coupled to the plurality of functional units and responsive to respective routing control signals for the plurality of unit level routing units, by which data is steered among the inputs and outputs of the plurality of functional units, unit level routing units in the plurality of unit level routing units being coupled to respective subsets of functional units in the plurality of functional unit, wherein at least one of said respective subsets of functional units is different that another of said respective subsets of functional units; (Fig. 1 , especially noting PE0 ... Pen, SP0 ... SPn and IOP0 ... IOPk, and col. 6 lines 39-51) *and*

functional unit level control word distribution circuitry which supplies control words for respective block function cycles to the plurality of unit level routing units, said control words including the routing control signals for the plurality of unit level routing units. (Fig. 10D in context of Fig. 1 #15, col. 6 lines 39-51)

Hillis, however, does not explicitly disclose:

... :

... ;

... *data is steered* ... ; *and*

... ;

... :

... ;

... ; *and*
... .

McMahon, though, discloses:

... :
... *data is steered* ... ; (Abstract) *and*
... ;
... :
... ;
... ; *and*
... .

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of McMahon for the benefit of Hillis, because to do so would have allowed a designer to improve microprocessor throughput, as taught by McMahon in col. 2 lines 15-24. These references were all applicable to the same field of endeavor, i.e., computer architecture.

Claims 13-21 are substantially similar to claims 2-10, respectively, and therefore likewise rejected.

Regarding claim 22, which is dependent upon claim 12, Hillis discloses:

> *wherein at least one of said block level control word distribution circuitry and functional level control word logic supplies distribution circuitry supplies said control words synchronously.* (Fig. 1 especially #15 and #17, col. 6 lines 36-38, and Fig. "11B-2E")

Regarding independent method claim 23, Hillis discloses:

A method of processing data, in a data processing engine that includes a plurality of functional units (Fig. 1), *comprising:*

providing a set of ... signals in parallel to a set of routing units in the data processing engine to specify a route among the plurality of functional units; (Fig. 1, col. 6 lines 35-38) *and*

routing data among the plurality of functional units according to the set of ... signals and performing tasks in the plurality of functional units using the route to produce a result, wherein routing units in the set of routing units are coupled to respective subsets of functional units in the plurality of functional units, wherein at least one of said respective subsets of functional units is different that another of said respective subsets of functional units. (Fig. 4A, Fig. 1 , especially noting PE0 ... Pen, SP0 ... SPn and IOP0 ... IOPk, and col. 6 lines 39-51)

Hillis, however, does not explicitly disclose:

... :

... *software routing control ... ; and*
... *software words routing control ... .*

McMahon, though, discloses:

... :

... *software routing control ... ;* (Abstract, Fig. 6) *and*
... *software words routing control ... .* (Abstract, Fig. 6)

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of McMahon for the benefit of Hillis, because to do so would have allowed a designer to improve microprocessor throughput, as taught by McMahon in col. 2 lines 15-24. These references were all applicable to the same field of endeavor, i.e., computer architecture.

Claims 25-26 are substantially similar to claims 9-10, respectively, and therefore likewise rejected.

Regarding claim 27, which is dependent upon claim 23, Hillis discloses:

> *wherein the routing units in the data processing engine comprise a plurality of switches interconnecting the plurality of functional units, ...* (Fig. 1 noting #11, 14 and 15)

Regarding claim 28, which is dependent upon claim 23, Hillis discloses:

> *including synchronously routing said data among the plurality of functional units.* (Fig. 1, and col. 6 lines 35-38 disclose the well-known concept of synchronous processing)

Regarding independent method claim 29, Hillis discloses:

A method of processing data, in a data processing engine that includes a plurality of functional units (Fig. 1),*comprising:*

providing a first set of ... signals in parallel to said set of routing units to specify a first data path according to a first configuration of the plurality of functional units, wherein routing units in the set of routing units are coupled to respective subsets of functional units in the plurality of functional units, wherein at least one of said respective subsets of functional units in the plurality of functional units, wherein at least one of said respective subsets of functional units is different that another of said respective subsets of functional units; (Fig. 1 , especially noting PE0 ... Pen, SP0 ... SPn and IOP0 ... IOPk, Abstract, and col. 6 lines 39-51)

performing tasks in said plurality of first functional units using the first data path; (Fig. 1, it being inherent that functional units must perform some task)

providing a second set of ... signals that in parallel to said set of routing units to specify a second data path according to a second configuration of the plurality of functional units, whereby the plurality of functional units is reconfigured to perform a different function; (Fig. 1 , especially noting PE0 ... Pen, SP0 ... SPn and IOP0 ... IOPk, Abstract, and col. 6 lines 39-51) *and*

performing tasks in said plurality of functional units using the second data path to accomplish said different function. (Fig. 1, it being inherent that functional units must perform some task)

Hillis, however, does not explicitly disclose:

... :
... *software routing control* ... ;
... ;
... *software routing control* ... ; *and*
... .

McMahon, though, discloses:

... :
... :
... *software routing control* ... ; (Abstract, Fig. 6)
... ;
... *software routing control* ... ; (Abstract, Fig. 6) *and*
... .

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of McMahon for the benefit of Hillis, because to do so would have allowed a designer to improve microprocessor throughput, as taught by McMahon in col. 2 lines 15-24. These references were all applicable to the same field of endeavor, i.e., computer architecture.

Claims 30-31 are substantially similar to claims 9-10, respectively, and therefore likewise rejected.

Claim 32 is substantially similar to claim 27, and therefore likewise rejected.

6. **Claims 24 and 33 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Hillis et al. (US Patent No. US 5,590,283, filed Jan. 27, 1995 and issued Dec. 31, 1996, hereafter

referred to as "Hillis") in view of McMahon (US Patent No. US 5,867,724, filed May 30, 1997 and issued Feb. 2, 1999, hereafter referred to as "McMahon") and further in view of Athanas et al. (US Patent No. 5,828,858, filed Sep. 16, 1996 and issued Oct. 27, 1998, hereafter referred to as "Athanas").

Regarding claim 24, which is dependent upon claim 23, the limitations of claim 23 have been previously discussed.

Hillis, however, does not explicitly disclose:

> *compiling a high level programming language specifying the result to produce the set of software words routing control signals.*

Athanas, though, discloses:

> *compiling a high level programming language specifying the result to produce the set of software words routing control signals.* (Fig. 7 and col. 10 line 59 – col. 11 line 10, esp. "compile time" and "library")

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Athanas for the benefit of Hillis in view of McMahon, because to do so would have allowed a computing system implementer to control large numbers of processors while facilitating data flows, as taught by Athanas in col. 1 lines 25-29. These references were all applicable to the same field of endeavor, i.e., computer architecture. Athanas was merely provided for its explicit teaching of the well-known concept of compilation.

Claim 33, which is dependent upon claim 29, is substantially similar to claim 24 and therefore likewise rejected.

Response to Arguments

7. It is respectfully noted that Applicant's amendment to the claims significantly changes the scope of the claimed invention as a whole. As such, much of Applicant's arguments (fax pages numbered 12-17 of the amendment) concerning FAOM rejections of claims 1-33 under 35 USC 103(a) have been rendered moot.

Applicant asserts on faxed pages 14-15 of 17 that the incorporation of well-known features such as parallel circuitry and messages/words/etc. containing an address field is novel.

The Office respectfully disagrees. The content of a data structure is merely a matter of obvious design choice. How one interconnects elements is a matter of limited design choice (i.e., in a serial or parallel fashion, each being obvious in light of the other).

Applicant also asserts on faxed page 16 of 17 that the Hillis reference does not teach the use of synchronous operation.

The Office respectfully disagrees. It is noted that Hillis does teach the use of a clock, a well-known architectural element for ensuring synchronous operation.

For at least these reasons, the Office raises the claim rejections under 35 USC 103(a) set forth above.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Non-Patent Literature

Arnold, Jeffrey, "The Splash 2 Software Environment", IDA Supercomputing Research Center, © 1993, [IEEE 0-816-3890-7/93], pp. 88-93.

US Patents

Nguyen et al	6,272,619
Morrisson et al	6,253,313
Tremblay et al	6,279,100
Baxter	6,182,206
Huang	4,943,909

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert M Stevens whose telephone number is (571) 272-4102. The examiner can normally be reached on M-F 6:00 - 2:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Heather R. Herndon can be reached on (571) 272-4136. The current fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Additionally, the main number for Technology Center 2100 is (571) 272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Robert M. Stevens
Reg. No. 47,972
Art Unit 2176
Date: April 16, 2005

rms

William L Bashore
WILLIAM BASHORE
PRIMARY EXAMINER
10/10/2005